

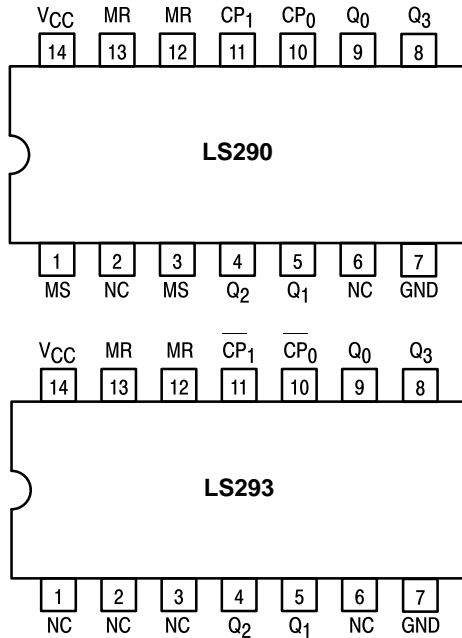


# DECADE COUNTER; 4-BIT BINARY COUNTER

The SN54/74LS290 and SN54/74LS293 are high-speed 4-bit ripple type counters partitioned into two sections. Each counter has a divide-by-two section and either a divide-by-five (LS290) or divide-by-eight (LS293) section which are triggered by a HIGH-to-LOW transition on the clock inputs. Each section can be used separately or tied together (Q to CP) to form BCD, Bi-quinary, or Modulo-16 counters. Both of the counters have a 2-input gated Master Reset (Clear), and the LS290 also has a 2-input gated Master Set (Preset 9).

- Corner Power Pin Versions of the LS90 and LS93
- Low Power Consumption . . . Typically 45 mW
- High Count Rates . . . Typically 42 MHz
- Choice of Counting Modes . . . BCD, Bi-Quinary, Binary
- Input Clamp Diodes Limit High Speed Termination Effects

### CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

### PIN NAMES

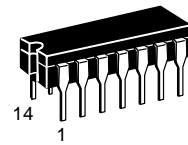
|            |  |
|------------|--|
| CP0        | Clock (Active LOW going edge) Input to +2 Section.         |
| CP1        | Clock (Active LOW going edge) Input to +5 Section (LS290). |
| CP1        | Clock (Active LOW going edge) Input to +8 Section (LS293). |
| MR1, MR2   | Master Reset (Clear) Inputs                                |
| MS1, MS2   | Master Set (Preset-9, LS290) Inputs                        |
| Q0         | Output from +2 Section (Notes b & c)                       |
| Q1, Q2, Q3 | Outputs from +5 & +8 Sections (Note b)                     |

### NOTES:

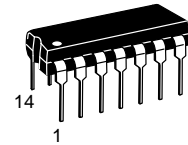
- a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.  
 b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.  
 c) The Q<sub>0</sub> Outputs are guaranteed to drive the full fan-out plus the CP<sub>1</sub> Input of the device.

**SN54/74LS290**  
**SN54/74LS293**

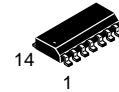
**DECADE COUNTER;  
4-BIT BINARY COUNTER**  
**LOW POWER SCHOTTKY**



**J SUFFIX**  
CERAMIC  
CASE 632-08



**N SUFFIX**  
PLASTIC  
CASE 646-06



**D SUFFIX**  
SOIC  
CASE 751A-02

### ORDERING INFORMATION

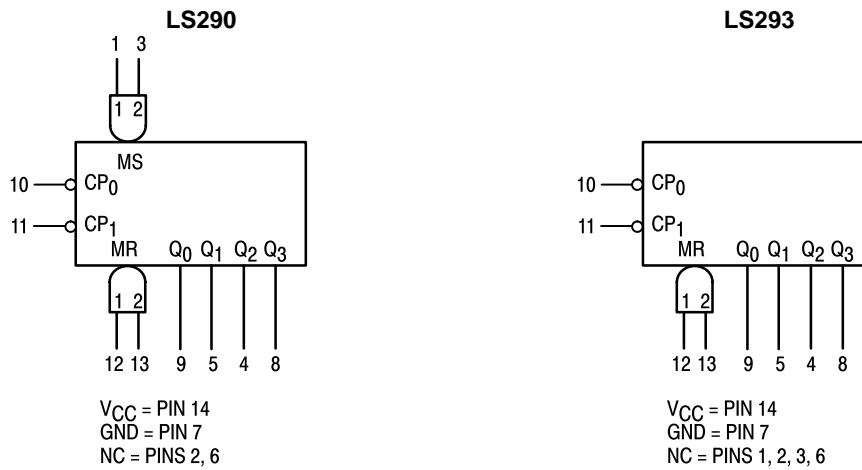
|            |         |
|------------|---------|
| SN54LSXXXJ | Ceramic |
| SN74LSXXXN | Plastic |
| SN74LSXXXD | SOIC    |

### LOADING (Note a)

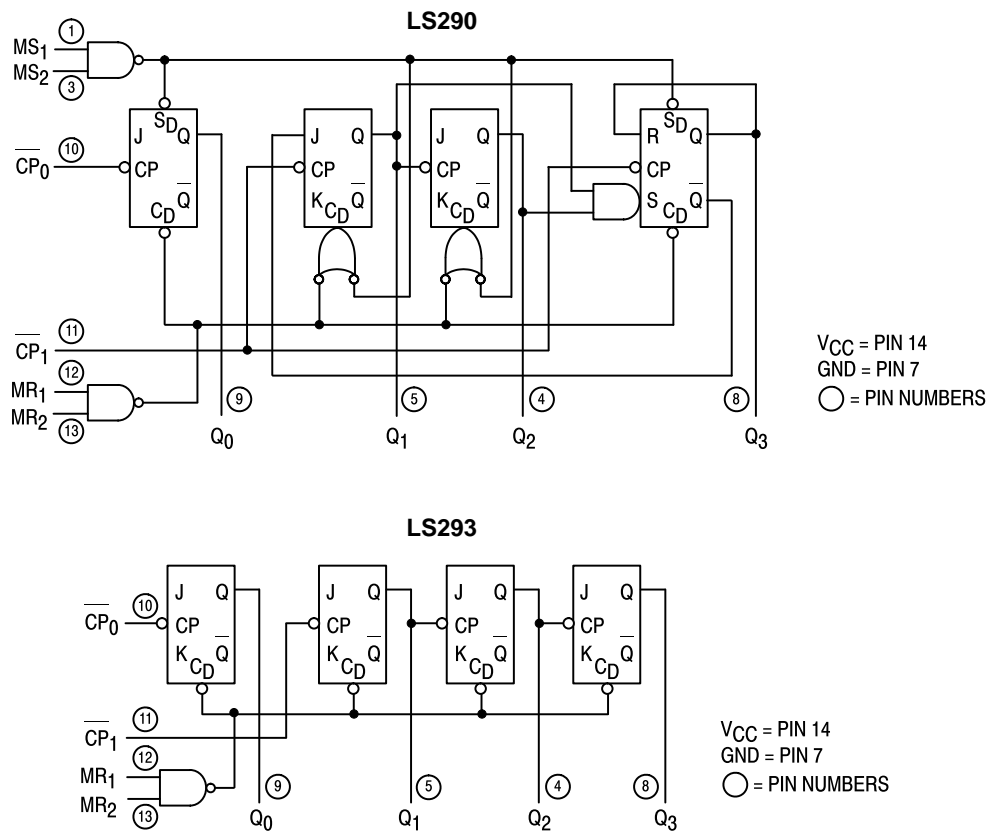
| HIGH      | LOW          |
|-----------|--------------|
| 0.05 U.L. | 1.5 U.L.     |
| 0.05 U.L. | 2.0 U.L.     |
| 0.05 U.L. | 1.0 U.L.     |
| 0.5 U.L.  | 0.25 U.L.    |
| 0.5 U.L.  | 0.25 U.L.    |
| 10 U.L.   | 5 (2.5) U.L. |
| 10 U.L.   | 5 (2.5) U.L. |

# SN54/74LS290 • SN54/74LS293

## LOGIC SYMBOL



## LOGIC DIAGRAMS



# SN54/74LS290 • SN54/74LS293

## FUNCTIONAL DESCRIPTION

The LS290 and LS293 are 4-bit ripple type Decade, and 4-Bit Binary counters respectively. Each device consists of four master/slave flip-flops which are internally connected to provide a divide-by-two section and a divide-by-five (LS290) or divide-by-eight (LS293) section. Each section has a separate clock input which initiates state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q<sub>0</sub> output of each device is designed and specified to drive the rated fan-out plus the CP<sub>1</sub> input of the device.

A gated AND asynchronous Master Reset (MR<sub>1</sub> · MR<sub>2</sub>) is provided on both counters which overrides the clocks and resets (clears) all the flip-flops. A gated AND asynchronous Master Set (MS<sub>1</sub> · MS<sub>2</sub>) is provided on the LS290 which overrides the clocks and the MR inputs and sets the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes:

### LS290

A. BCD Decade (8421) Counter — the CP<sub>1</sub> input must be

externally connected to the Q<sub>0</sub> output. The CP<sub>0</sub> input receives the incoming count and a BCD count sequence is produced.

- B. Symmetrical Bi-quinary Divide-By-Ten Counter — The Q<sub>3</sub> output must be externally connected to the CP<sub>0</sub> input. The input count is then applied to the CP<sub>1</sub> input and a divide-by-ten square wave is obtained at output Q<sub>0</sub>.
- C. Divide-By-Two and Divide-By-Five Counter — No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function (CP<sub>0</sub> as the input and Q<sub>0</sub> as the output). The CP<sub>1</sub> input is used to obtain binary divide-by-five operation at the Q<sub>3</sub> output.

### LS293

A. 4-Bit Ripple Counter — The output Q<sub>0</sub> must be externally connected to input CP<sub>1</sub>. The input count pulses are applied to input CP<sub>0</sub>. Simultaneous division of 2, 4, 8, and 16 are performed at the Q<sub>0</sub>, Q<sub>1</sub>, Q<sub>2</sub>, and Q<sub>3</sub> outputs as shown in the truth table.

B. 3-Bit Ripple Counter — The input count pulses are applied to input CP<sub>1</sub>. Simultaneous frequency divisions of 2, 4, and 8 are available at the Q<sub>1</sub>, Q<sub>2</sub>, and Q<sub>3</sub> outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

LS290 MODE SELECTION

| RESET/SET INPUTS |                 |                 |                 | OUTPUTS        |                |                |                |
|------------------|-----------------|-----------------|-----------------|----------------|----------------|----------------|----------------|
| MR <sub>1</sub>  | MR <sub>2</sub> | MS <sub>1</sub> | MS <sub>2</sub> | Q <sub>0</sub> | Q <sub>1</sub> | Q <sub>2</sub> | Q <sub>3</sub> |
| H                | H               | L               | X               | L              | L              | L              | L              |
| H                | H               | X               | L               | L              | L              | L              | L              |
| X                | X               | H               | H               | H              | L              | L              | H              |
| L                | X               | L               | X               |                |                | Count          |                |
| X                | L               | X               | L               |                |                | Count          |                |
| L                | X               | X               | L               |                |                | Count          |                |
| X                | L               | L               | X               |                |                | Count          |                |

LS293 MODE SELECTION

| RESET INPUTS    |                 | OUTPUTS        |                |                |                |
|-----------------|-----------------|----------------|----------------|----------------|----------------|
| MR <sub>1</sub> | MR <sub>2</sub> | Q <sub>0</sub> | Q <sub>1</sub> | Q <sub>2</sub> | Q <sub>3</sub> |
| H               | H               | L              | L              | L              | L              |
| L               | H               |                |                | Count          |                |
| H               | L               |                |                | Count          |                |
| L               | L               |                |                | Count          |                |

LS290  
BCD COUNT SEQUENCE

| COUNT | OUTPUT         |                |                |                |
|-------|----------------|----------------|----------------|----------------|
|       | Q <sub>0</sub> | Q <sub>1</sub> | Q <sub>2</sub> | Q <sub>3</sub> |
| 0     | L              | L              | L              | L              |
| 1     | H              | L              | L              | L              |
| 2     | L              | H              | L              | L              |
| 3     | H              | H              | L              | L              |
| 4     | L              | L              | H              | L              |
| 5     | H              | L              | H              | L              |
| 6     | L              | H              | H              | L              |
| 7     | H              | H              | H              | L              |
| 8     | L              | L              | L              | H              |
| 9     | H              | L              | L              | H              |

NOTE: Output Q<sub>0</sub> is connected to Input CP<sub>1</sub> for BCD count.

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care

TRUTH TABLE

| COUNT | OUTPUT         |                |                |                |
|-------|----------------|----------------|----------------|----------------|
|       | Q <sub>0</sub> | Q <sub>1</sub> | Q <sub>2</sub> | Q <sub>3</sub> |
| 0     | L              | L              | L              | L              |
| 1     | H              | L              | L              | L              |
| 2     | L              | H              | L              | L              |
| 3     | H              | H              | L              | L              |
| 4     | L              | L              | H              | L              |
| 5     | H              | L              | H              | L              |
| 6     | L              | H              | H              | L              |
| 7     | H              | H              | H              | L              |
| 8     | L              | L              | L              | H              |
| 9     | H              | L              | L              | H              |
| 10    | L              | H              | L              | H              |
| 11    | H              | H              | L              | H              |
| 12    | L              | L              | H              | H              |
| 13    | H              | L              | H              | H              |
| 14    | L              | H              | H              | H              |
| 15    | H              | H              | H              | H              |

Note: Output Q<sub>0</sub> connected to input CP<sub>1</sub>.

# SN54/74LS290 • SN54/74LS293

## GUARANTEED OPERATING RANGES

| Symbol          | Parameter                           |          | Min         | Typ        | Max         | Unit |
|-----------------|-------------------------------------|----------|-------------|------------|-------------|------|
| V <sub>CC</sub> | Supply Voltage                      | 54<br>74 | 4.5<br>4.75 | 5.0<br>5.0 | 5.5<br>5.25 | V    |
| T <sub>A</sub>  | Operating Ambient Temperature Range | 54<br>74 | -55<br>0    | 25<br>25   | 125<br>70   | °C   |
| I <sub>OH</sub> | Output Current — High               | 54, 74   |             |            | -0.4        | mA   |
| I <sub>OL</sub> | Output Current — Low                | 54<br>74 |             |            | 4.0<br>8.0  | mA   |

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

| Symbol          | Parameter  | Limits |       |      | Unit | Test Conditions  |   |
|-----------------|--|--------|-------|------|------|--|---|
|                 |  | Min    | Typ   | Max  |      |  |   |
| V <sub>IH</sub> | Input HIGH Voltage   | 2.0    |       |      | V    | Guaranteed Input HIGH Voltage for All Inputs   |   |
| V <sub>IL</sub> | Input LOW Voltage  | 54     |       | 0.7  | V    | Guaranteed Input LOW Voltage for All Inputs  |   |
|                 |  | 74     |       | 0.8  |      |  |   |
| V <sub>IK</sub> | Input Clamp Diode Voltage  |        | -0.65 | -1.5 | V    | V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA  |   |
| V <sub>OH</sub> | Output HIGH Voltage  | 54     | 2.5   | 3.5  | V    | V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table |   |
|                 |  | 74     | 2.7   | 3.5  | V    |  |   |
| V <sub>OL</sub> | Output LOW Voltage   | 54, 74 |       | 0.25 | 0.4  | V  | I <sub>OL</sub> = 4.0 mA<br>V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table |
|                 |  | 74     |       | 0.35 | 0.5  | V  |   |
| I <sub>IH</sub> | Input HIGH Current   |        |       | 20   | μA   | V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V   |   |
|                 |  |        |       | 0.1  | mA   | V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V   |   |
| I <sub>IL</sub> | Input LOW Current<br>MS, MR<br>CP <sub>0</sub><br>CP <sub>1</sub> (LS290)<br>CP <sub>1</sub> (LS293) |        |       | -0.4 | mA   | V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V   |   |
|                 |  |        |       | -2.4 |      |  |   |
|                 |  |        |       | -3.2 |      |  |   |
|                 |  |        |       | -1.6 |      |  |   |
| I <sub>OS</sub> | Short Circuit Current (Note 1)   | -20    |       | -100 | mA   | V <sub>CC</sub> = MAX  |   |
| I <sub>CC</sub> | Power Supply Current   |        |       | 15   | mA   | V <sub>CC</sub> = MAX  |   |

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

# SN54/74LS290 • SN54/74LS293

**AC CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5.0\text{ V}$ ,  $C_L = 15\text{ pF}$ )

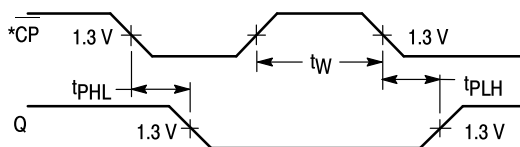
| Symbol                               | Parameter  | Limits |          |          |       |          |          | Unit |
|--------------------------------------|--|--------|----------|----------|-------|----------|----------|------|
|                                      |  | LS290  |          |          | LS293 |          |          |      |
|                                      |  | Min    | Typ      | Max      | Min   | Typ      | Max      |      |
| $f_{\text{MAX}}$                     | CP <sub>0</sub> Input Clock Frequency                                | 32     |          |          | 32    |          |          | MHz  |
| $f_{\text{MAX}}$                     | CP <sub>1</sub> Input Clock Frequency                                | 16     |          |          | 16    |          |          | MHz  |
| $t_{\text{PLH}}$<br>$t_{\text{PHL}}$ | Propagation Delay,<br>CP <sub>0</sub> Input to Q <sub>0</sub> Output |        | 10<br>12 | 16<br>18 |       | 10<br>12 | 16<br>18 | ns   |
| $t_{\text{PLH}}$<br>$t_{\text{PHL}}$ | CP <sub>0</sub> Input to Q <sub>3</sub> Output                       |        | 32<br>34 | 48<br>50 |       | 46<br>46 | 70<br>70 | ns   |
| $t_{\text{PLH}}$<br>$t_{\text{PHL}}$ | CP <sub>1</sub> Input to Q <sub>1</sub> Output                       |        | 10<br>14 | 16<br>21 |       | 10<br>14 | 16<br>21 | ns   |
| $t_{\text{PLH}}$<br>$t_{\text{PHL}}$ | CP <sub>1</sub> Input to Q <sub>2</sub> Output                       |        | 21<br>23 | 32<br>35 |       | 21<br>23 | 32<br>35 | ns   |
| $t_{\text{PLH}}$<br>$t_{\text{PHL}}$ | CP <sub>1</sub> Input to Q <sub>3</sub> Output                       |        | 21<br>23 | 32<br>35 |       | 34<br>34 | 51<br>51 | ns   |
| $t_{\text{PHL}}$                     | MS Input to Q <sub>0</sub> and Q <sub>3</sub> Outputs                |        | 20       | 30       |       |          |          | ns   |
| $t_{\text{PHL}}$                     | MS Input to Q <sub>1</sub> and Q <sub>2</sub> Outputs                |        | 26       | 40       |       |          |          | ns   |
| $t_{\text{PHL}}$                     | MR Input to Any Output   |        | 26       | 40       |       | 26       | 40       | ns   |

**AC SETUP REQUIREMENTS** ( $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5.0\text{ V}$ )

| Symbol           | Parameter                   | Limits |     |       |     | Unit |
|------------------|-----------------------------|--------|-----|-------|-----|------|
|                  |                             | LS290  |     | LS293 |     |      |
|                  |                             | Min    | Max | Min   | Max |      |
| $t_W$            | CP <sub>0</sub> Pulse Width | 15     |     | 15    |     | ns   |
| $t_W$            | CP <sub>1</sub> Pulse Width | 30     |     | 30    |     | ns   |
| $t_W$            | MS Pulse Width              | 15     |     |       |     | ns   |
| $t_W$            | MR Pulse Width              | 15     |     | 15    |     | ns   |
| $t_{\text{rec}}$ | Recovery Time MR to CP      | 25     |     | 25    |     | ns   |

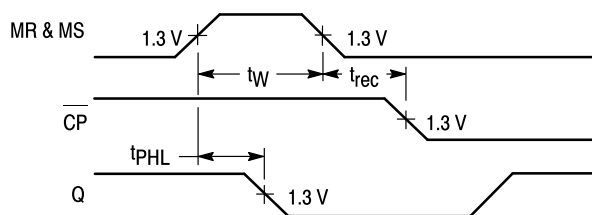
RECOVERY TIME ( $t_{\text{rec}}$ ) is defined as the minimum time required between the end of the reset pulse and the clock transition from HIGH-to-LOW in order to recognize and transfer HIGH data to the Q outputs.

### AC WAVEFORMS

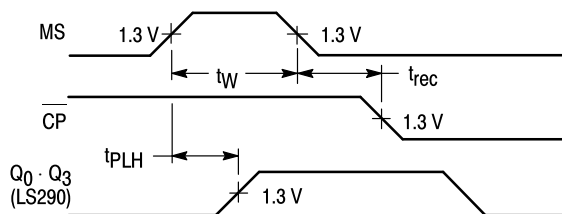


**Figure 1**

\*The number of Clock Pulses required between the  $t_{\text{PHL}}$  and  $t_{\text{PLH}}$  measurements can be determined from the appropriate Truth Tables.

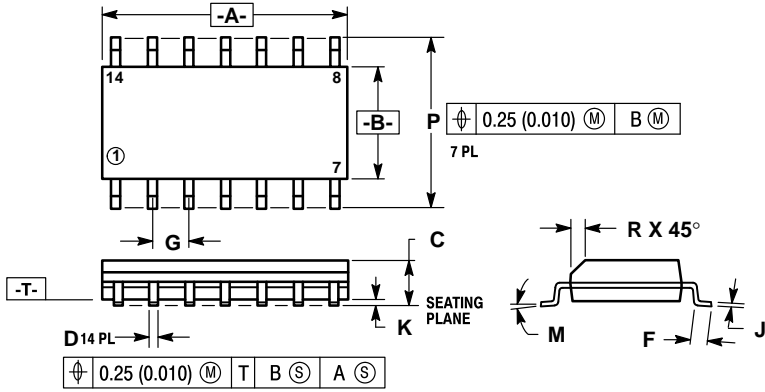


**Figure 2**



**Figure 3**

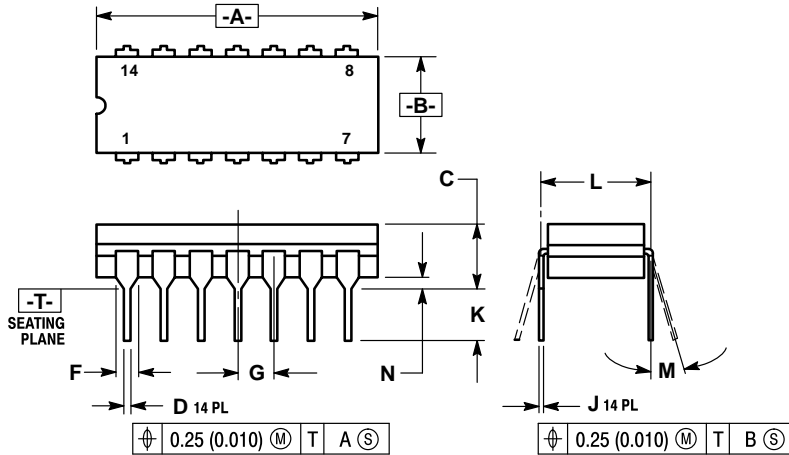
**Case 751A-02 D Suffix  
14-Pin Plastic  
SO-14**



- NOTES:
1. DIMENSIONS "A" AND "B" ARE DATUMS AND "T" IS A DATUM SURFACE.
  2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  3. CONTROLLING DIMENSION: MILLIMETER.
  4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  6. 751A-01 IS OBSOLETE, NEW STANDARD 751A-02.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 8.55        | 8.75 | 0.337     | 0.344 |
| B   | 3.80        | 4.00 | 0.150     | 0.157 |
| C   | 1.35        | 1.75 | 0.054     | 0.068 |
| D   | 0.35        | 0.49 | 0.014     | 0.019 |
| F   | 0.40        | 1.25 | 0.016     | 0.049 |
| G   | 1.27 BSC    |      | 0.050 BSC |       |
| J   | 0.19        | 0.25 | 0.008     | 0.009 |
| K   | 0.10        | 0.25 | 0.004     | 0.009 |
| M   | 0°          | 7°   | 0°        | 7°    |
| P   | 5.80        | 6.20 | 0.229     | 0.244 |
| R   | 0.25        | 0.50 | 0.010     | 0.019 |

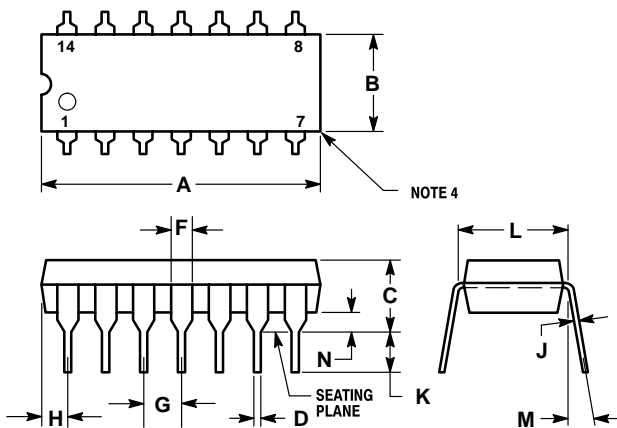
**Case 632-08 J Suffix  
14-Pin Ceramic Dual In-Line**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
  4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.
  5. 632-01 THRU -07 OBSOLETE, NEW STANDARD 632-08.


| DIM | MILLIMETERS |       | INCHES    |       |
|-----|-------------|-------|-----------|-------|
|     | MIN         | MAX   | MIN       | MAX   |
| A   | 19.05       | 19.94 | 0.750     | 0.785 |
| B   | 6.23        | 7.11  | 0.245     | 0.280 |
| C   | 3.94        | 5.08  | 0.155     | 0.200 |
| D   | 0.39        | 0.50  | 0.015     | 0.020 |
| F   | 1.40        | 1.65  | 0.055     | 0.065 |
| G   | 2.54 BSC    |       | 0.100 BSC |       |
| J   | 0.21        | 0.38  | 0.008     | 0.015 |
| K   | 3.18        | 4.31  | 0.125     | 0.170 |
| L   | 7.62 BSC    |       | 0.300 BSC |       |
| M   | 0°          | 15°   | 0°        | 15°   |
| N   | 0.51        | 1.01  | 0.020     | 0.040 |

**Case 646-06 N Suffix  
14-Pin Plastic**



- NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
  2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
  3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
  4. ROUNDED CORNERS OPTIONAL.
  5. 646-05 OBSOLETE, NEW STANDARD 646-06.

| DIM | MILLIMETERS |       | INCHES    |       |
|-----|-------------|-------|-----------|-------|
|     | MIN         | MAX   | MIN       | MAX   |
| A   | 18.16       | 19.56 | 0.715     | 0.770 |
| B   | 6.10        | 6.60  | 0.240     | 0.260 |
| C   | 3.69        | 4.69  | 0.145     | 0.185 |
| D   | 0.38        | 0.53  | 0.015     | 0.021 |
| F   | 1.02        | 1.78  | 0.040     | 0.070 |
| G   | 2.54 BSC    |       | 0.100 BSC |       |
| H   | 1.32        | 2.41  | 0.052     | 0.095 |
| J   | 0.20        | 0.38  | 0.008     | 0.015 |
| K   | 2.92        | 3.43  | 0.115     | 0.135 |
| L   | 7.62 BSC    |       | 0.300 BSC |       |
| M   | 0°          | 10°   | 0°        | 10°   |
| N   | 0.39        | 1.01  | 0.015     | 0.039 |

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